REMARKS

Favorable reconsideration of this application, in light of the following discussion and in view of the present amendment, is respectfully requested.

Claims 1, 6, 14, 19 and 20 are amended. Claims 1-20 are pending in the present application.

Entry of Amendment under 37 C.F.R. § 1.116

The Applicant requests entry of this Rule 116 Response because: the amendments were not earlier presented because the Applicant believed in good faith that the cited references did not disclose the present invention as previously claimed; and the amendment does not significantly alter the scope of the claim and places the application at least into a better form for purposes of appeal.

The Manual of Patent Examining Procedures (M.P.E.P.) sets forth in Section 714.12 that "any amendment that would place the case either in condition for allowance or in better form for appeal may be entered." Moreover, Section 714.13 sets forth that "the Proposed Amendment should be given sufficient consideration to determine whether the claims are in condition for allowance and/or whether the issues on appeal are simplified." The M.P.E.P. further articulates that the reason for any non-entry should be explained expressly in the Advisory Action.

I. Information Disclosure Statement

The Examiner noted that the Information Disclosure Statement fails to comply with the provisions of 37 C.F.R. 1.97, 1.98 and MPEP § 609. The Applicant respectfully requests reconsideration of the Information Disclosure Statement filed January 26, 2006, as Document numbers 10-330531 (Korea), 10-335504 (Korea) and 10-358628 (Korea) were submitted with the remaining cited foreign patent documents. To clarify, the publication numbers are different from the initial document numbers cited and were identified in the IDS according to the initial document numbers in order to remain consistent with the previously submitted document numbers. Specifically, publication number 2000-53529 is consistent with document number 10-330531, publication number 2002-3015 is consistent with document number 10-335504, and publication number 2001-6816 is consistent with document number 10-358628.

An Information Disclosure Statement complying with 37 C.F.R. 1.97, 1.98 and MPEP § 609 is filed concurrently with the Amendment to the present application, resubmitting the three references discussed above.

II. Rejection under 35 U.S.C. § 102

In the Office Action, at page 4, numbered paragraph 7, claims 6-9, 14, 16-17 and 19 were rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 6,003,121 to Wirt. This rejection is respectfully traversed because Wirt does not discuss or suggest:

> a controller determining whether the plurality of the memory buses operate in the multi-channel mode by comparing memory information of at least one of a plurality of memory modules of a first channel to at least one of a plurality of memory modules of at least a second channel, the memory modules being connected to the respective memory buses, to make a determination as to whether characteristics of at least one of the memory modules of the first channel are compatible with characteristics of at least one of the memory modules of the second channel such that the memory buses can operate in the multi-channel mode; and
>
> an output unit providing information about whether the plurality of memory buses operate in the multi-channel mode according to the determination by the controller,

as recited in amended independent claim 6, and similarly in amended independent claims 14 and 19.

As a non-limiting example, the present invention as set forth in claim 6, for example, is directed to a computer including a plurality of channel memory buses which are connected to a memory controller in parallel. At least a first channel and a second channel include a plurality of memory modules which are connected to the first and the second channel memory bus. Memory information of the memory modules is compared to determine whether the characteristics of at least one of the memory modules of the first channel and at least one of the memory modules of the second channel are compatible so that the memory buses can operate in a multi-channel mode.

Wirt discusses that RDRAM device characteristics are read and a determination is made as to whether the device characteristics have previously been read. If the characteristics have not been previously read, the RDRAMs device and group IDs are programmed based upon current device and group counters and the device and group counters are incremented. If the characteristics have previously been read, a determination is made as to whether the group having those device characteristics is full and if not, the RDRAM group ID is programmed to have the same ID as that group having the same characteristics. If the group is full, a determination is made as to whether there are other empty groups with the same characteristics (col. 3, lines 10-39). Wilt does not, however, discuss or suggest that it is determined whether plural memory buses operate in the multi-channel mode by comparing memory information of

one of the memory modules of a first channel to at least one of a plurality of memory modules of at least a second channel to determine whether the characteristics of a memory module of the first channel are compatible with the characteristics of a memory module of the second channel so that the memory buses can operate in the multi-channel mode and outputting information about whether the memory buses operate in the multi-channel mode according to the determination. Wirt merely discusses grouping devices based on the characteristics of the devices that are read, but does not discuss or suggest that a determination about memory buses operating in multi-channel mode is made based on a comparison between the characteristics of the memory modules of the first and second channels. The present invention looks at characteristics of the memory modules to determine the compatibility between memory modules of different channels to decide whether the memory buses can operate in the multi-channel mode. Wirt discusses grouping RDRAMs according to their characteristics where a RIMM module may have more than one Direct RDRAM Channel, but in which all the RDRAMs on any given channel have the same characteristics (col. 3, lines 47-52), but Wirt does not does discuss or suggest that a determination is made as to whether the memory buses can operate in the multi-channel mode based on a comparison between the compatibility of the characteristics of memory modules of separate channels.

Therefore, as Wirt does not discuss or suggest "determining whether the plurality of the memory buses operate in the multi-channel mode by comparing memory information of at least one of a plurality of memory modules of a first channel to at least one of a plurality of memory modules of at least a second channel, the memory modules being connected to the respective memory buses, to make a determination as to whether characteristics of at least one of the memory modules of the first channel are compatible with characteristics of at least one of the memory modules of the second channel such that the memory buses can operate in the multi-channel mode," as recited in amended independent claim 6, and similarly in amended independent claims 14 and 19, claims 6, 14 and 19 patentably distinguish over the reference relied upon. Accordingly, withdrawal of the § 102(b) rejection is respectfully requested.

Claims 7-9 and 16-17 depend either directly or indirectly from amended independent claims 6 and 14 and include all the features of claims 6 and 14, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 9 recites that "the controller examines an existence of an arrangement of the memory modules connected to the plurality of the memory buses that allows the plurality of the memory buses to operate in the multi-channel mode, when the controller determines that the plurality of the memory buses do not operate in the multi-channel mode." Therefore, claims 7-9 and 16-17 patentably distinguish

over the reference relied upon for at least the reasons noted above. Accordingly, withdrawal of the § 102(b) rejection is respectfully requested.

III. Rejections under 35 U.S.C. § 103

In the Office Action, at page 9, numbered paragraph 8, claims 1-13, 17 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wirt in view of U.S. Patent No. 6,845,277 B1 to Michelet et al. This rejection is respectfully traversed.

As discussed above with respect to independent claims 6, 14 and 19, Wirt does not discuss or suggest "a controller determining whether the plurality of the memory buses operate in the multi-channel mode by comparing memory information of at least one of a plurality of memory modules of a first channel to at least one of a plurality of memory modules of at least a second channel, the memory modules being connected to the respective memory buses, to make a determination as to whether characteristics of at least one of the memory modules of the first channel are compatible with characteristics of at least one of the memory modules of the second channel such that the memory buses can operate in the multi-channel mode." Further, with respect to independent claims 1 and 20, and in a similar argument to that above with respect to claims 6, 14 and 19, Wirt does not discuss or suggest "displaying whether the plurality of the memory buses operate in the multi-channel mode by comparing the read memory information of a first memory module of a first channel to the read memory information of at least a second memory module of at least a second channel to make a determination as to whether characteristics of the first memory module of the first channel are compatible with characteristics of at least one of the memory modules of the second channel such that the memory buses can operate in the multi-channel mode," as recited in amended independent claim 1 and similarly in amended independent claim 20.

While Michelet discusses a hardware monitoring process having on screen display capabilities, Michelet does not make up for the deficiency in Wirt, with respect to the newly amended portions of independent claims 1, 6 and 20. Specifically, Michelet does not discuss or suggest making a determination as to whether characteristics of the first memory module of the first channel are compatible with characteristics of at least one of the memory modules of the second channel such that the memory buses can operate in the multi-channel mode. Therefore, as the combination of Wirt and Michelet does not suggest all the claim limitations of independent claims 1, 6 and 20, as is necessary in establishing a *prima facie* case of obviousness, claims 1, 6 and 20 patentably distinguish over the references relied upon. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Claims 2-5, 7-13 and 17 depend either directly or indirectly from independent claims 1 and 6 and include all the features of claims 1 and 6, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 5 recites that "the displaying whether the plurality of the memory buses operate in the multi-channel mode further comprises displaying the arrangement of the memory modules allowing the plurality of the memory buses to operate in the multi-channel mode." Therefore, claims 2-5 patentably distinguish over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Wirt in view of Kawamata

In the Office Action, at page 16, numbered paragraph 9, claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Wirt in view of U.S. Patent No. 6,535,420 B1 to Kawamata. This rejection is respectfully traversed.

As discussed above with respect to amended independent claim 14, Wirt does not teach or suggest "comparing the read memory information of at least one of the memory modules of the first channel to the read memory information of at least one of the memory modules of at least the second channel to make a determination as to whether characteristics of at least one of the memory modules of the first channel are compatible with characteristics of at least one of the memory modules of the second channel such that the memory buses can operate in the multi-channel mode." Kawamata, which discusses only that a storage area is able to store information such as manufacturer information, fails to make up for the deficiencies in Wirt, specifically in determining the compatibility of characteristics of memory modules in separate channels to determine that memory buses can operate in the multi-channel mode, as recited in amended independent claim 14. Claim 15 depends directly from independent claim 14 and includes all the features of claim 14, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 15 recites that "the memory information comprises manufacturer information, device structure and logical bank information, type information and capacity information." Therefore, claim 15 patentably distinguishes over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Wirt in view of Cepulis

In the Office Action, at page 17, numbered paragraph 10, claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Wirt in view of U.S. Patent No. 6,496,945 B2 to Cepulis et al.

As discussed above with respect to amended independent claim 6, Wirt does not teach or suggest "a controller determining whether the plurality of the memory buses operate in the multi-channel mode by comparing memory information of at least one of a plurality of memory modules of a first channel to at least one of a plurality of memory modules of at least a second channel, the memory modules being connected to the respective memory buses, to make a determination as to whether characteristics of at least one of the memory modules of the first channel are compatible with characteristics of at least one of the memory modules of the second channel such that the memory buses can operate in the multi-channel mode." Cepulis, which discusses only that a computer system implements fault detection isolation technique that tracks failed physical devices by identification (ID) codes embedded in each component of the computer, fails to make up for the deficiencies in Wirt, specifically in determining the compatibility of characteristics of memory modules in separate channels to determine that memory buses can operate in the multi-channel mode, as recited in amended independent claim 6. Claim 18 depends indirectly from independent claim 6 and includes all the features of claim 6, plus additional features that are not discussed or suggested by the references relied upon. For example, claim 18 recites "a north bridge controlling the plurality of the memory modules, wherein the controller controls the north bridge to read the memory information during the POST." Therefore, claim 18 patentably distinguishes over the references relied upon for at least the reasons noted above. Accordingly, withdrawal of the § 103(a) rejection is respectfully requested.

Conclusion

In accordance with the foregoing, claims 1, 6, 14, 19 and 20 have been amended. Claims 1-20 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 9/15/06

By: _____

Kari P. Footland
Registration No. 55,187

1201 New York Avenue, NW, 7th Floor
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501